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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Brian R. Mears et al.

Title: MULTIPLE CHANNEL INTERFACE FOR COMMUNICATIONS BETWEEN DEVICES

Docket No.: 884.481US1
Filed: September 21, 2001
Examiner: Nimesh G. Patel

Serial No.: 09/961,024
Due Date: June 12, 2006
Group Art Unit: 2112

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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Amy Moriarty
Name

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Brian R. Mears et al. Examiner: Nimesh G. Patel

Serial No.: 09/961,024 Group Art Unit: 2112

Filed: September 21, 2001 Docket: 884.481US1

For: MULTIPLE CHANNEL INTERFACE FOR COMMUNICATIONS BETWEEN DEVICES

Assignee: Intel Corporation

APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on April 12, 2006, from the Final Rejection of claims 1-14, 16-18, 28-31, 33-44, and 49 of the above-identified application, as set forth in the Final Office Action mailed on January 12, 2006.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, INTEL CORPORATION.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings known to the appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 1-14, 16-18, 28-31, 33-44, and 49 were rejected under 35 USC §103(a), and these claims rejected under 35 USC §103(a) are being appealed.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the final office action dated January 12, 2006.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 recites a communications interface (12, 14, page 4, lines 3-4) including a bus interface (300, page 5, line 1) coupleable to an internal bus (110, page 3, line 27), a plurality of transmit channels (306, page 5, line 4) coupled to the bus interface, a transmit control block (308, page 5, line 7) coupled to the plurality of transmit channels, a plurality of outbound links (116, page 5, line 8) coupled to a plurality of outputs of the transmit control block, a plurality of receive channels (310, page 5, line 9) coupled to the bus interface; a receive control block (312, page 5, line 10) coupled to the plurality of receive channels, and a plurality of inbound links (118, page 4, lines 5-6) coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface. The communications interface also includes a stop message (page 13, line 21) channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO (316, page 13, line 20) reaches a stop threshold value (page 13, line 19) and a start message (page 13, line 25) channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value (page 13, line 19).

Claim 28 recites a method of transmitting data between semiconductor chips including writing data into at least one of a plurality of transmit FIFOs (314, page 5, lines 23-24), selecting one of the plurality of transmit FIFOs that contains data to be transmitted and that is not in a wait state, transmitting the data to a corresponding one of a plurality of receive FIFOs (316, page 5, line 12) that has not exceeded a threshold value (page 13, line 21), sending a stop message (page 13, line 21) if the corresponding one of the receive FIFOs cannot receive data, and sending a start message (page 13, line 25) when the corresponding one of the receive FIFOs can receive data.

Claim 36 recites a method of forming a communications interface including forming a bus interface (300, page 5, line 1), forming a plurality of transmit channels (306, page 5, line 4) coupled to the bus interface, forming a transmit control block (308,

page 5, line 7) coupled to the plurality of transmit channels, forming a plurality of outbound links (116, page 5, line 8) coupled to a plurality of outputs of the transmit control block, forming a plurality of receive control channels (310, page 5, line 9) coupled to the bus interface, forming a receive control block (312, page 5, line 10) coupled to the plurality of receive control channels, and forming a plurality of inbound links (118, page 4, lines 5-6) coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface. The method also includes forming a stop message (page 13, line 21) channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO (316, page 5, line 12) reaches a stop threshold value, and forming a start message (page 13, line 25) channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

Claim 44 recites a method including supplying a clock signal (1314, page 16, lines 8-9) from a first terminal, supplying a strobe signal (1310, page 16, line 6) from a second terminal, providing an identification value (1108, page 18, lines 5-6) corresponding to a selected channel register from data terminals when the strobe signal is active, providing data from the selected channel register at the data terminals (1-7, page 18, line 10) when the strobe signal is inactive, the data changing in accordance with the clock signal, and providing a third terminal that receives a wait signal (1308, page 17, line 26) that keeps the data provided at the data terminals from changing. The method also includes providing a stop message (1502, page 18, line 11) channel (channel E, page 18, line 12) coupled to the receive control block (312, page 5, line 10) and adapted to send a stop message to a source when a receive FIFO (316, page 5, line 12) reaches a stop threshold value and providing a start message (1504, page 18, line 23) channel (channel F, page 18, line 24)coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and the appellants refer to the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1-14, 16-18, 28-31, 33-34, 36-44, and 49 were rejected under 35 USC § 103(a) as being unpatentable over Baker (U.S. 6,333,938) in view of Earnest (U.S. 6,226,338).

II. Claim 35 was rejected under 35 USC § 103(a) as being unpatentable over Baker (U.S. 6,333,938) in view of Earnest (U.S. 6,226,338) and Holm et al. (U.S. 6,122,680, Holm).

7. ARGUMENT

The Applicable Law

All of the pending claims were rejected under 35 U.S.C. §103:

> "A patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art."[1]

Factual findings must be set out to support a rejection under 35 USC §103:

> "In order to determine obviousness as a legal matter, four factual inquiries must be made concerning: 1) the scope and content of the prior art; 2) the level of ordinary skill in the art; 3) the differences between the claimed invention and the prior art; and 4) secondary considerations."[2]

The MPEP states the following with regard to rejections under 35 USC §103:

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. "[3]

The appellants respectfully submit that the final Office Action fails to make a *prima facie* showing of obviousness by failing to show motivation to combine the applied references, and also fails to provide evidence of a reasonable expectation of success of each of the combinations of references.

A Federal Circuit opinion states that the suggestion or motivation to combine references and the reasonable expectation of success must both be found in the prior art.[4]

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[1] 35 U.S.C. § 103(a).
[2] *Ruiz v. A.B. Chance Co.*, 57 USPQ2d 1161, 1165 (Fed. Cir. 2000) citing *Graham v. John Deere Co.*, 148 USPQ 459 (1966).
[3] MPEP 2143.
[4] MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

Multiple Federal Circuit decisions emphasize the need for the PTO to furnish evidence in support of claim rejections. For example, the Federal Circuit addressed citation of "basic knowledge or common sense" in rejections in *In re Zurko*:

> "With respect to core factual findings in a determination of patentability, however, the Board [Board of Patent Appeals and Interferences] cannot simply reach conclusions based on its own understanding or experience – or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings."[5]

The Federal Circuit has particularly emphasized the need for the PTO to furnish evidence in support of claim rejections under 35 USC § 103 in *In re Lee*:

> "When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness.....The factual inquiry whether to combine references must be thorough and searching....It must be based on objective evidence of record." [6]

The Federal Circuit stated that the "need for specificity pervades this authority" requiring a teaching, motivation, or suggestion to select and combine references.[7] The Federal Circuit has expressed this need for specificity in several cases:

> "[T]he best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.....the showing must be clear and particular." [8]

> "[E]ven when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination."[9]

> "[P]articular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed."[10]

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[5] *In re Zurko*, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001).
[6] *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).
[7] *In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).
[8] *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).
[9] *In re Rouffet*, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998).
[10] *In re Kotzab*, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

A finding of a suggestion or motivation is part of the inquiry into the scope and content of the prior art under *Graham*:

> "Determining whether there is a suggestion or motivation to modify a prior art reference is one aspect of determining the scope and content of the prior art, a fact question subsidiary to the ultimate conclusion of obviousness."[11]

Official notice should only be used where the facts asserted are capable of instant and unquestionable demonstration:

> "the Patent Office...may take notice of facts beyond the record which, while not generally notorious, are capable of such instant and unquestionable demonstration as to defy dispute."[12]

The "state of the art" is not an appropriate subject of official notice:

> "[W]e reject the notion that judicial or administrative notice may be taken of the state of the art. The facts constituting the state of the art are normally subject to the possibility of rational disagreement among reasonable men and are not amendable to the taking of such notice."[13]

Official notice should rarely be used in a final office action:

> "While 'official notice' may be relied on, these circumstances should be rare when an application is under final rejection."[14]

Reliance on a reference to support a ground of rejection that is not included in the statement of the rejection is impermissible according to *In re Hoch*[15] and *Ex parte Raske*.[16]

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[11] *Ruiz v. A.B. Chance Co.*, 57 USPQ2d 1161, 1167 (Fed. Cir. 2000).
[12] *In re Ahlert*, 165 USPQ 418, 420 (CCPA 1970).
[13] *In re Eynde*, 178 USPQ 470, 474 (CCPA 1973).
[14] MPEP 2144.03.
[15] *In re Hoch*, 166 USPQ 406, 407 n.3 (CCPA 1970).
[16] *Ex parte Raske*, 28 USPQ2d 1304, 1304-05 (Bd. Pat. App. & Int. 1993).

I. Claims 1-14, 16-18, 28-31, 33-34, 36-44, and 49 were rejected under 35 USC § 103(a) as being unpatentable over Baker (U.S. 6,333,938) in view of Earnest (U.S. 6,226,338). The appellants respectfully traverse.

Baker relates to a PCI-interface device.[17] Baker shows in Figure 2 "the functional partitioning of PCI-interface ASIC 20."[18] Baker shows and describes the PCI-interface ASIC 20 in detail.[19]

Earnest relates to a "multiple-channel data communication buffer" that "includes a transmit first-in-first-out ("FIFO") circuit and a receive FIFO circuit."[20] Earnest describes a receive FIFO 18 in detail,[21] and the final Office Action proposes to add the "FULL" flag of the receive FIFO 18 of Earnest[22] to the PCI-interface ASIC 20 of Baker.

The final office action has not shown evidence from the prior art of a suggestion to one skilled in the art to combine Baker and Earnest, and has not shown evidence of a reasonable expectation of success. Finally, Baker and Earnest do not show all of the features recited in the claims.

No Evidence of a Suggestion or Motivation to Combine

The final office action states with respect to claim 1:

> "Baker does not specifically disclose a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value....it would have been obvious to include the stop message channel, as disclosed by Earnest, in the system of Baker, since this would prevent the writing of data in FIFO that has no more room for data."[23]

[17] Baker, Abstract.
[18] Baker, column 5, lines 66-67.
[19] Baker, column 5, line 66 to column 13, line 15.
[20] Earnest, Abstract.
[21] Earnest, column 9, line 37, to column 11, line 55.
[22] Earnest, column 11, lines 40-45.
[23] Final Office Action, page 3.

Similar statements are made in other parts of the rejection with respect to claims 28, 36, and 44.[24] The final office action has not identified prior art as being the source of the above-quoted rationale for combining Baker and the buffer of Earnest as is required by MPEP 2143. The devices and methods described in Baker are specifically directed to extracting control information from packetized data in an IEEE 1394 standard or similar PCI interface device.[25] The final office action has not shown why a skilled person would be motivated to modify the system of Baker that complies with IEEE 1394. The final office action has not shown evidence that the system of Baker that is compliant with IEEE 1394 is deficient in a way that can be remedied by addition of the "FULL" flag of the receive FIFO 18 of Earnest.

The advisory action dated 3 April 2006 stated the source of the above-quoted rationale for combining Baker and the buffer of Earnest is "knowledge generally available to one of ordinary skill in the art." The appellants respectfully submit that even if the rationale is not found in the applied references, the final office action must show that the rationale came from the prior art with some other evidence to satisfy *In re Lee* and *In re Vaeck.*

No Evidence of a Reasonable Expectation of Success

The final Office Action also lacks evidence from the prior art of a reasonable expectation of success of this combination of Baker and Earnest as required by MPEP 2143. The final Office Action has not shown where the "FULL" flag of the receive FIFO 18 of Earnest is to be added to the system of Baker. Baker describes the PCI-interface ASIC 20 in detail, and the final Office Action has not shown where in the detailed ASIC 20 of Baker the "FULL" flag of the receive FIFO 18 of Earnest is to be added. The PCI-interface ASIC 20 of Baker complies with IEEE 1394.[26] The final Office Action has not shown that the buffer of Earnest is compliant with IEEE 1394. The final Office Action

[24] Final Office Action, pages 6-7, 8, and 10-11.
[25] Baker, column 3, lines 5-11.
[26] Baker, column 5, lines 27-35.

has not shown how the system of Baker that is compliant with IEEE 1394 can be modified by elements of Earnest and still maintain compliance with IEEE 1394. The final office action has not set forth this required element of a *prima facie* case of obviousness.

Traverse of Official Notice

The final office action states with respect to claim 7:

> "Official Notice is being taken that advantages of power management are well known in the art and it would have been obvious to include a power management unit in the system of Baker since this would allow power to be saved."[27]

The appellants respectfully traverse this assertion of official notice. Official notice is taken of supposed "advantages of power management." The final office action appears to be taking official notice that a claimed feature is obvious. Official notice cannot be used to establish obviousness when *Graham* requires a factual inquiry and *In re Lee* and *In re Vaeck* demand a showing of evidence to support the legal conclusion. Official notice should only be used where the facts asserted are capable of instant and unquestionable demonstration according to *In re Ahlert*. The "state of the art" is not an appropriate subject of official notice according to *In re Eynde*. Official notice should rarely be used in a final office action. See MPEP 2144.03.

[27] Final Office Action, page 4.

MPEP 2144.03 cites both *In re Zurko* and *In re Lee* requiring that rejections be based on evidence of record.[28]

The advisory action lists four new references, Fung, Gulick, Dahlen, and Vernon et al., purporting to be evidence of the notoriety of power management and the round robin algorithm. Fung, Gulick, Dahlen, and Vernon et al. are not discussed in this brief because they are not included in the statement of the ground of rejection in the final office action dated 12 January 2006. Reliance on a reference to support a ground of rejection that is not included in the statement of the rejection is impermissible according to *In re Hoch*[29] and *Ex parte Raske.*[30] The appellants respectfully submit that Fung, Gulick, Dahlen, and Vernon et al. cannot be relied on to support this ground of rejection.

The appellants respectfully submit that the official notice taken in the final Office action is improper under MPEP 2144.03, should be withdrawn, and that the affected claims are in condition for allowance.

Individual Claims

Claim 4 recites a long list of different registers. For example, claim 4 recites an interface width register, an end of message register, a wait count register, etc... The final office points out only a transmit FIFO and a status register in Baker. The other features recited in claim 4 are not identified in the final office action as being shown in Baker or Earnest.

Claim 5 recites a long list of different registers. For example, claim 5 recites an interface width register, an end of message register, a wake up register, etc... The final office points out only a receive FIFO and a status register in Baker. The other features recited in claim 5 are not identified in the final office action as being shown in Baker or Earnest.

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[28] *In re Zurko*, 59 USPQ2d 1693 (Fed. Cir. 2001); *In re Lee*, 61 USPQ2d 1430 (Fed. Cir. 2002).
[29] *In re Hoch*, 166 USPQ 406, 407 n.3 (CCPA 1970).
[30] *Ex parte Raske*, 28 USPQ2d 1304, 1304-05 (Bd. Pat. App. & Int. 1993).

Claim 7 recites "a power management unit coupled to each of the plurality of transmit channels and receive channels." The final office action admits that Baker does not show a power management unit, but takes official notice of same. The appellants respectfully traverse this assertion of official notice as discussed above.

Claim 16 recites "at least one of a direct flow control mode and a message flow control to control a flow of data across the communications interface." The final office action pointed to column 19, lines 7-15 of Baker, and this text does not discuss the direct flow control mode or the message flow control recited in claim 16. These features recited in claim 16 are not identified in the final office action as being shown in Baker or Earnest.

Claim 30 recites "selecting another one of the plurality of transmit FIFOs to send data to another corresponding one of the plurality of receive FIFOs while the corresponding one of the receive FIFOs cannot receive data." The final office action pointed to Baker, column 14, lines 20-28 which do not discuss this feature recited in claim 30. These features recited in claim 30 are not identified in the final office action as being shown in Baker or Earnest.

Claim 34 recites that "the predetermined algorithm is round-robin" and was rejected with the following sentence:

> "Regarding claim 34, Baker does not disclose the predetermined algorithm is round-robin. However, the round-robin algorithm is a well-known arbitration scheme and therefore could be substituted for the arbitration scheme in Baker's system."[31]

The final office action admits that Baker is missing the "round-robin" feature, but does not point to any prior art with the feature. None of the elements of a *prima facie* case of obviousness of MPEP 2143 are established in this rejection of claim 34. This

[31] Final office action, page 7.

feature recited in claim 34 is not identified in the final office action as being shown in Baker or Earnest.

The appellants respectfully submit that a *prima facie* case of obviousness of claims 1-14, 16-18, 28-31, 33-34, 36-44, and 49 has not been established in the final office action.

II. Claim 35 was rejected under 35 USC § 103(a) as being unpatentable over Baker (U.S. 6,333,938) in view of Earnest (U.S. 6,226,338) and Holm et al. (U.S. 6,122,680, Holm). The appellants respectfully traverse.

Claim 35 is rejected based on a combination of three references: Baker, Earnest, and Holm. MPEP 2143 requires a suggestion and a reasonable expectation of success for each combination of references. In other words, MPEP 2143 requires two layers of motivation, and two layers of reasonable expectation of success, to combine three references under §103. The final office action has not shown evidence of a motivation to combine Baker with Earnest or evidence of a reasonable expectation of success of this combination. Additionally, the final office action is missing evidence of a motivation to combine Holm with Baker and Earnest, and evidence of a reasonable expectation of success of this combination.

Holm relates to a "multiple channel data communication buffer."[32] The final office action states:

> "it would have been obvious to use the teachings of Holm in the system of Baker and Earnest, to use a bus with varying width since this would increase compatibility."[33]

The final office action has not identified prior art as being the source of the above-quoted rationale for combining Baker, Earnest, and Holm as is required by *In re Lee* and *In re Vaeck*. The final office action has not presented prior art showing a reasonable expectation of success of such an arrangement.

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[32] Holm, Abstract.
[33] Final Office Action, page 11.

The appellants respectfully submit that a *prima facie* case of obviousness of claim 35 has not been established in the final office action.

8. SUMMARY

Request For Reversal

For the foregoing reasons, the appellants respectfully submit that the rejections of claims 1-14, 16-18, 28-31, 33-44, and 49 under 35 U.S.C. §103 were erroneous. Reversal of these rejections is respectfully requested.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

BRIAN R. MEARS et al.

By their Representatives,

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Date 12 JUNE 2006 By _____
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Amy Moriarty
Name

_____
Signature

CLAIMS APPENDIX

1. (Rejected) A communications interface, comprising:

a bus interface coupleable to an internal bus;

a plurality of transmit channels coupled to the bus interface;

a transmit control block coupled to the plurality of transmit channels;

a plurality of outbound links coupled to a plurality of outputs of the transmit control block;

a plurality of receive channels coupled to the bus interface; and

a receive control block coupled to the plurality of receive channels; and

a plurality of inbound links coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface; and

a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value; and

a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

2. (Rejected) The communications interface of claim 1, further comprising a direct memory access controller coupled to the bus interface.

3. (Rejected) The communications interface of claim 1, wherein the bus interface comprises a plurality of transmit control registers and a plurality of receive control registers.

4. (Rejected) The communications interface of claim 3, wherein the plurality of transmit control registers comprises at least one of:

an interface width register coupled to the transmit control block;

a transmit first in first out (FIFO) register associated with each transmit channel;

an end of message (EOM) register associated with each transmit channel;

an interface interrupt identification register coupled to the transmit control block;

a transmit frequency select register coupled to the transmit control block;

a wait count register coupled to the transmit control block;

a clock stop time register coupled to the transmit control block;

a channel configuration register associated with each transmit channel; and

a channel status register associated with each transmit channel.

5. (Rejected) The communications interface of claim 3, wherein the plurality of receive control registers comprises at least one of:

a receive FIFO register coupled to each receive channel;

an interface width register to select a predetermined number of bits to be received across the communications interface by the receive control block;

a channel stop register associated with each receive channel;

a channel start register associated with each receive channel;

a wake up register associated with at least one receive channel;

an end of message register associated with each receive channel;

a channel configuration register associated with each receive channel; and

a channel status register associated with each receive channel.

6. (Rejected) The communications interface of claim 1, wherein each of the plurality of transmit channels and each of the plurality of receive channels comprises a first in first out (FIFO) memory device.

7. (Rejected) The communications interface of claim 1, further comprising a power management unit coupled to each of the plurality of transmit channels and receive channels.

8. (Rejected) The communications interface of claim 1, wherein the transmit control block comprises a channel arbiter adapted to select a next one of the plurality of transmit channels to be activated.

9. (Rejected) The communications interface of claim 1, wherein the transmit control block comprises a link controller adapted to transmit data from a selected transmit channel across a selected link.

10. (Rejected) The communications interface of claim 1, wherein the receive control block comprises a state machine adapted to store a current active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels.

11. (Rejected) The communications interface of claim 1, wherein the plurality of transmit channels comprises:

at least one channel adapted to send a clock signal;
at least one channel adapted to send a strobe signal;
at least one channel adapted to send a wait signal; and
at least one channel adapted to send data.

12. (Rejected) The communications interface of claim 1, wherein the plurality of receive channels comprises:

at least one channel adapted to send a clock signal;
at least one channel adapted to send a strobe signal;
at least one channel adapted to send a wait signal; and

at least one channel adapted to send data.

13. (Rejected) The communications interface of claim 1, wherein at least one of the plurality of transmit channels and the plurality of receive channels comprise a virtual general purpose input/output channel.

14. (Rejected) The communications interface of claim 1, further comprising:

a channel stop threshold register adapted to set the stop threshold value to cause the stop message to be sent to the source when the receive FIFO is full; and

a channel start threshold register adapted to set the start threshold value to cause the start message to be sent to the source when the receive FIFO can receive additional data.

15. (Canceled)

16. (Rejected) The communications interface of claim 1, further comprising at least one of a direct flow control mode and a message flow control to control a flow of data across the communications interface.

17. (Rejected) The communications interface of claim 1, wherein the transmit control block comprises:

a multiplexer coupled to the plurality of transmit channels;

a parallel in serial out converter (PISO) coupled to the multiplexer; and

a control circuit coupled to the multiplexer and the PISO and adapted to select one of the plurality of transmit channels to transmit data.

18. (Rejected) The communications interface of claim 1, wherein the receive control block comprises:

a demultiplexer coupled to the plurality of receive channels;

a serial in parallel out converter (SIPO); and

a control circuit coupled to the demultiplexer and adapted to select one of the plurality of receive channels to receive data.

19 - 27. (Canceled)

28. (Rejected) A method of transmitting data between semiconductor chips, comprising:

writing data into at least one of a plurality of transmit FIFOs;

selecting one of the plurality of transmit FIFOs that contains data to be transmitted and that is not in a wait state; and

transmitting the data to a corresponding one of a plurality of receive FIFOs that has not exceeded a threshold value; and

sending a stop message if the corresponding one of the receive FIFOs cannot receive data; and

sending a start message when the corresponding one of the receive FIFOs can receive data.

29. (Rejected) The method of claim 28, further comprising:

sending a wait signal to a transmit control block if the corresponding one of the receive FIFOs cannot receive data; and

removing the wait signal when the corresponding one of the receive FIFOs can receive data; and

sending a stop message if the corresponding one of the receive FIFOs cannot receive data; and

sending a start message when the corresponding one of the receive FIFOs can receive data.

30. (Rejected) The method of claim 28, further comprising selecting another one of the plurality of transmit FIFOs to send data to another corresponding one of the plurality of receive FIFOs while the corresponding one of the receive FIFOs cannot receive data.

31. (Rejected) The method of claim 28, further comprising:

sending a strobe signal to initiate a transmission of data;

sending a selected channel number over which the data is to be transmitted; and

sending an end of message signal after the data has been transmitted.

32. (Canceled)

33. (Rejected) The method of claim 28, further comprising:

selecting one of the plurality of transmit FIFOs and the corresponding one of the plurality of receive FIFOs by a predetermined algorithm.

34. (Rejected) The method of claim 28, wherein the predetermined algorithm is round-robin.

35. (Rejected) The method of claim 28, further comprising selecting a interface width from one of a serial width, a two-bit width and a nibble width.

36. (Rejected) A method of forming a communications interface, comprising:

forming a bus interface;

forming a plurality of transmit channels coupled to the bus interface;

forming a transmit control block coupled to the plurality of transmit channels;

forming a plurality of outbound links coupled to a plurality of outputs of the transmit control block;

forming a plurality of receive control channels coupled to the bus interface;

forming a receive control block coupled to the plurality of receive control channels; and

forming a plurality of inbound links coupled to a plurality of inputs of the receive control block, the inbound links and the outbound links to couple the bus interface to a further bus interface; and

forming a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value; and

forming a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

37. (Rejected) The method of claim 36, wherein forming the bus interface comprises forming a plurality of transmit control registers and a plurality of receive control registers.

38. (Rejected) The method of claim 36, wherein forming the transmit control block comprises:

forming a channel arbiter adapted to determine a next one of the plurality of channels to be activated; and

forming a link controller adapted to transmit data from a selected transmit channel across a selected link.

39. (Rejected) The method of claim 36, wherein forming the receive control block comprises forming a state machine adapted to store a currently active channel number, a number of bits in a current byte being transferred and to write each byte to a selected one of the plurality of receive channels.

40. (Rejected) The method of claim 36, wherein forming the plurality of transmit channels and forming the plurality of receive channels, each comprises:

forming at least one channel adapted to send a clock signal;

forming at least one channel adapted to send a strobe signal;

forming at least one channel adapted to send a wait signal; and

forming at least one channel adapted to send data.

41. (Rejected) The method of claim 36, further comprising forming at least one virtual general purpose input/output channel.

42. (Rejected) The method of claim 36, wherein forming the transmit control block comprises:

forming a multiplexer coupled to the plurality of transmit channels;

forming a parallel in serial out converter (PISO) coupled to the multiplexer; and

forming a control circuit coupled to the multiplexer and to the PISO.

43. (Rejected) The method of claim 36, wherein forming the receive control block comprises:

forming a demultiplexer coupled to the plurality of receive channels;

forming a serial in parallel out converter (SIPO);

forming a control circuit coupled to the demultiplexer and adapted to select one of the plurality of receive channels to receive data.

44. (Rejected) A method, comprising:

supplying a clock signal from a first terminal;

supplying a strobe signal from a second terminal;

providing an identification value corresponding to a selected channel register from data terminals when the strobe signal is active;

providing data from the selected channel register at the data terminals when the strobe signal is inactive, the data changing in accordance with the clock signal; and

providing a third terminal that receives a wait signal that keeps the data provided at the data terminals from changing; and

providing a stop message channel coupled to the receive control block and adapted to send a stop message to a source when a receive FIFO reaches a stop threshold value; and

providing a start message channel coupled to the receive control block and adapted to send a start message to the source when the receive FIFO reaches a start threshold value.

45. - 48. (Canceled)

49. (Rejected) The communications interface of claim 1, further comprising:

a channel stop threshold register to store the stop threshold value to cause the stop message to be sent to the source when an amount of data in the receive FIFO exceeds the stop threshold value; and

a channel start threshold register to store the start threshold value to cause the start message to be sent to the source when an amount of data in the receive FIFO falls below the start threshold value.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.